WHAT IS CLAIMED IS:

1. An oversampling modulator device comprising:

an addition unit outputting an signal indicating a sum of an input signal and a first delayed signal, the input signal having a plurality of bits, the output signal divided into a first signal having a number of upper bits of the output signal and a second signal having the remaining bits of the output signal;

a subtraction unit outputting a signal indicating a difference between the first signal from the addition unit and a second delayed signal;

a first delay unit outputting the first delayed signal to the addition unit by delaying a third signal having upper bits produced by the output signal of the subtraction unit and lower bits produced by the second signal from the addition unit;

a quantization unit performing quantization processing of the third signal and outputting a quantization signal having a predetermined number of bits; and

a second delay unit outputting the second delayed signal to the subtraction unit by delaying the quantization signal,

wherein the quantization unit selects specific bits included in the third signal and generates the quantization signal with the selected bits of the third signal.

2. The oversampling modulator device of claim 1 wherein the quantization unit is provided to perform the quantization processing in a limited range between an upper limit and a lower limit for data indicated by the input signal, and comprises an overflow circuit outputting a signal indicating the upper limit when the data is larger than the upper limit, and an underflow circuit outputting a signal indicating the lower limit when the

data is smaller than the lower limit.

3. The oversampling modulator device of claim 1 further comprising a multiplication unit receiving an output signal of the second delay unit and generating the second delayed signal as an output to the subtraction unit by computing an integral multiple of the received signal.

4. An oversampling modulator device comprising:

a subtraction unit outputting an signal indicating a difference between a first signal and a first delayed signal, the first signal having a number of upper bits included in an input signal, the input signal having a plurality of bits and being divided into the first signal and a second signal;

an addition unit outputting a signal indicating a sum of a third signal and a second delayed signal, the third signal having upper bits produced by the output signal of the subtraction unit and lower bits produced by the second signal having the remaining bits of the input signal;

a quantization unit performing quantization processing of the output signal of the addition unit and outputting a quantization signal having a predetermined number of bits;

a first delay unit outputting the first delayed signal to the subtraction unit by delaying the quantization signal from the quantization unit; and

a second delay unit outputting the second delayed signal to the addition unit by delaying the output signal of the addition unit,

wherein the quantization unit selects specific bits included in the output signal of the addition unit and generates the quantization signal with the selected bits of the output signal of

the addition unit.

5. The oversampling modulator device of claim 4 wherein the quantization unit is provided to perform the quantization processing in a limited range between an upper limit and a lower limit for data indicated by the input signal, and comprises an overflow circuit outputting a signal indicating the upper limit when the data is larger than the upper limit, and an underflow circuit outputting a signal indicating the lower limit when the data is smaller than the lower limit.

6. The oversampling modulator device of claim 4 further comprising a multiplication unit receiving an output signal of the first delay unit and generating the second delayed signal as an output to the subtraction unit by computing an integral multiple of the received signal.

7. The oversampling modulator device of claim 1 wherein the quantization unit comprises signal lines corresponding to the specific bits in the third signal, and buffers connected to the signal lines, the quantization unit outputting the quantization signal from the buffers.

8. The oversampling modulator device of claim 1 wherein the quantization unit comprises: signal lines corresponding to

the specific bits in the third signal; a plurality of first logical elements connected to the signal lines; and a second logical element receiving a signal indicating a sign of the data indicated by the input signal.

9. The oversampling modulator device of claim 4 wherein the quantization unit comprises signal lines corresponding to the specific bits in the third signal, and buffers connected to the signal lines, the quantization unit outputting the quantization signal from the buffers.

10. The oversampling modulator device of claim 4 wherein the quantization unit comprises: signal lines corresponding to the specific bits in the third signal; a plurality of first logical elements connected to the signal lines; and a second logical element receiving a signal indicating a sign of the data indicated by the input signal.